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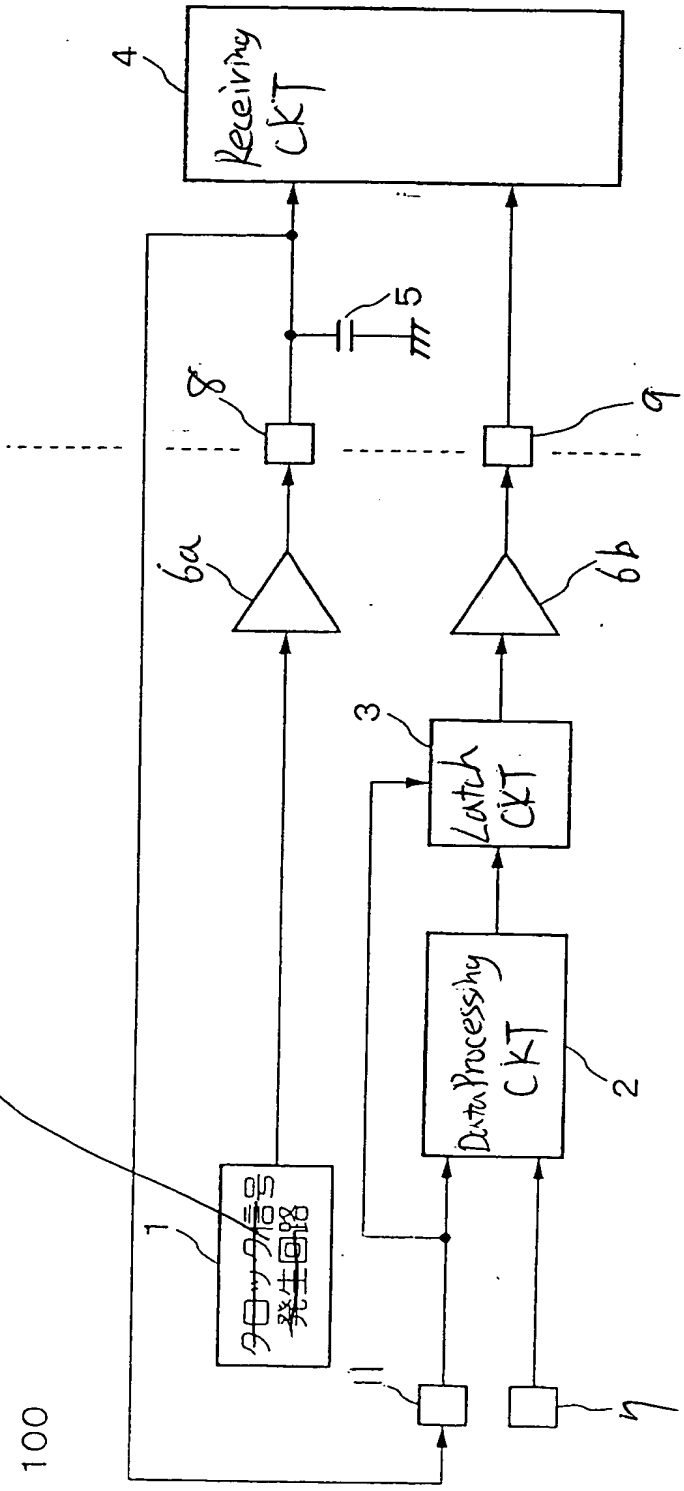
【書類名】　図面

【図１】

FIG 1



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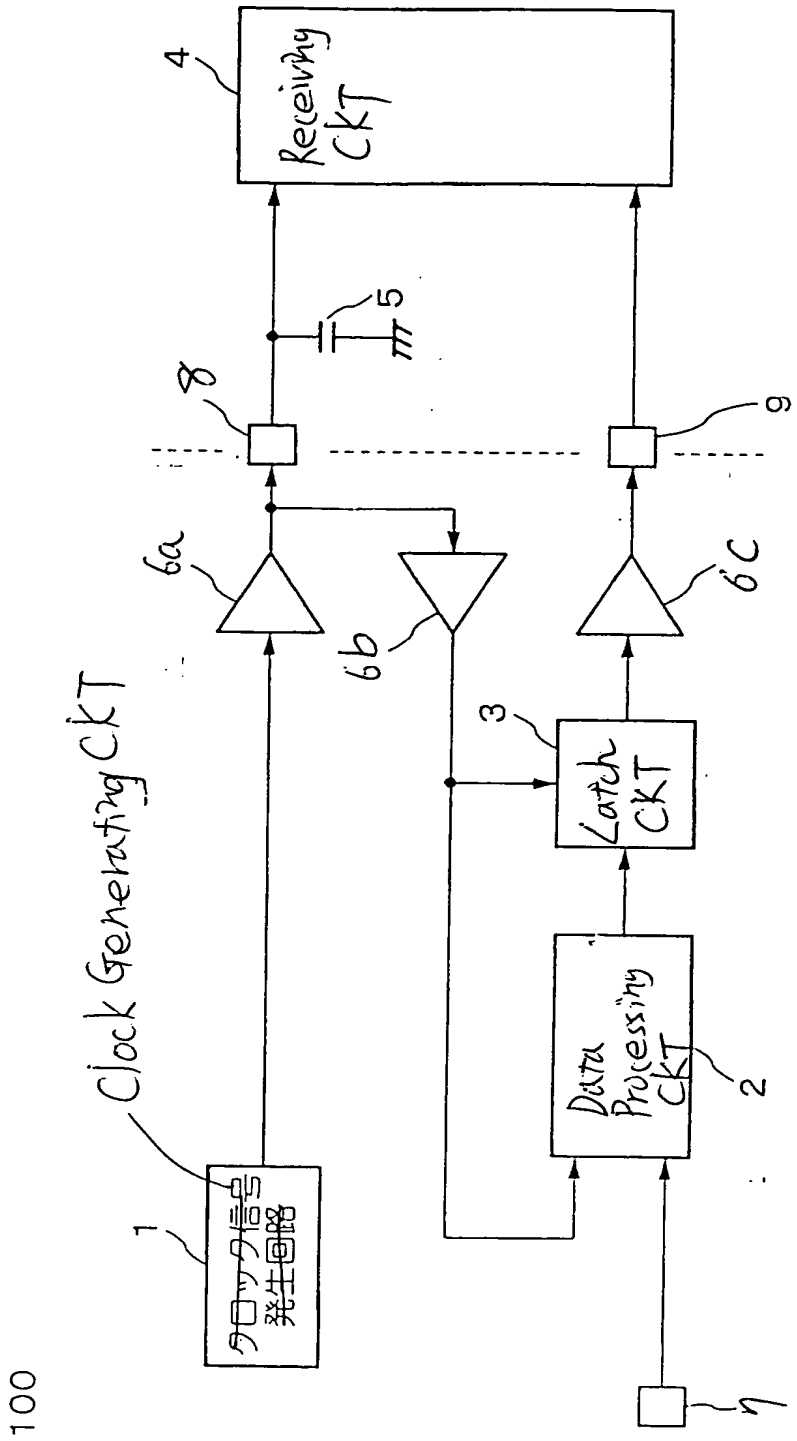
~~【図2】~~

FIG. 2



~~【図3】~~

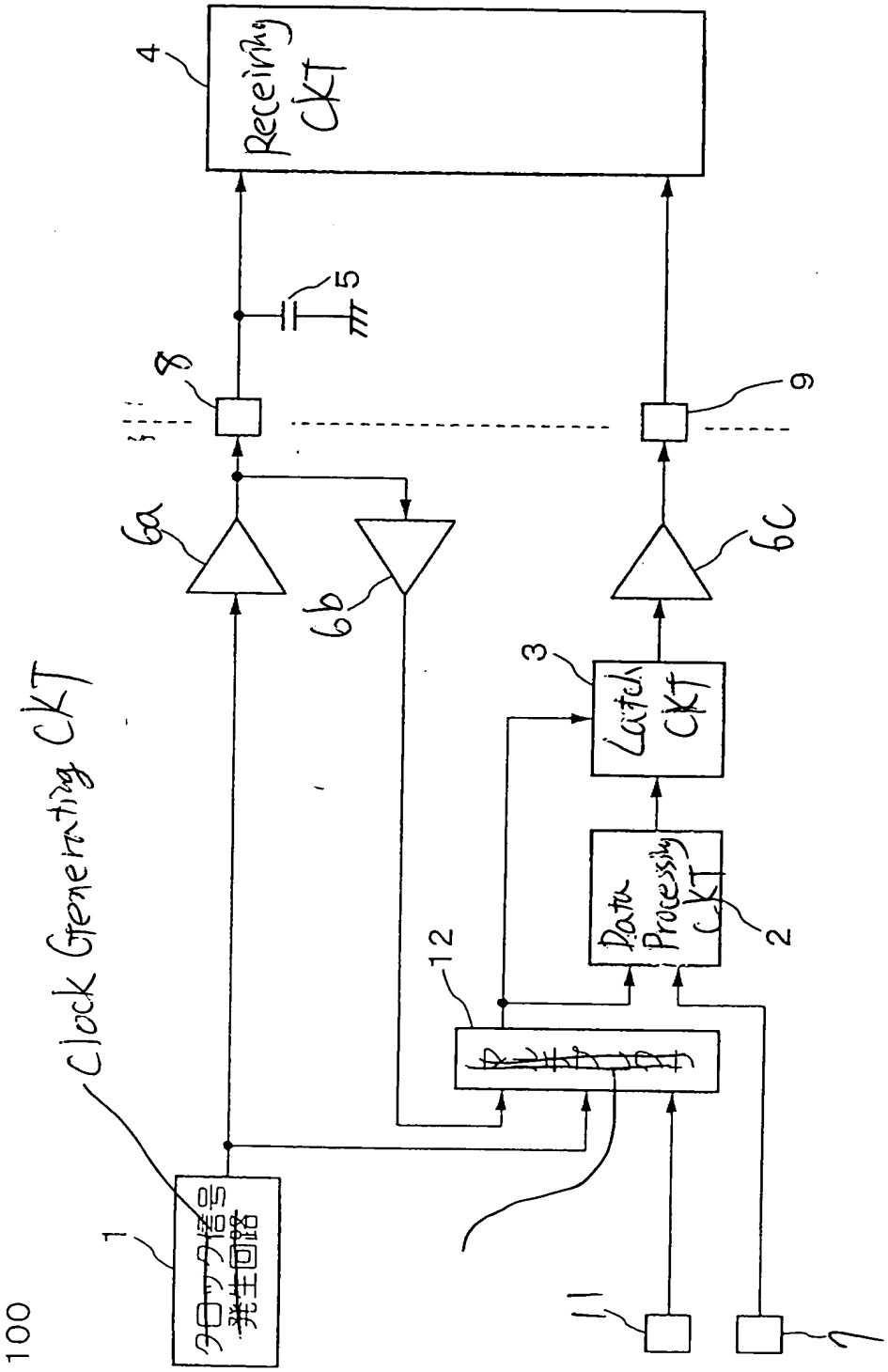
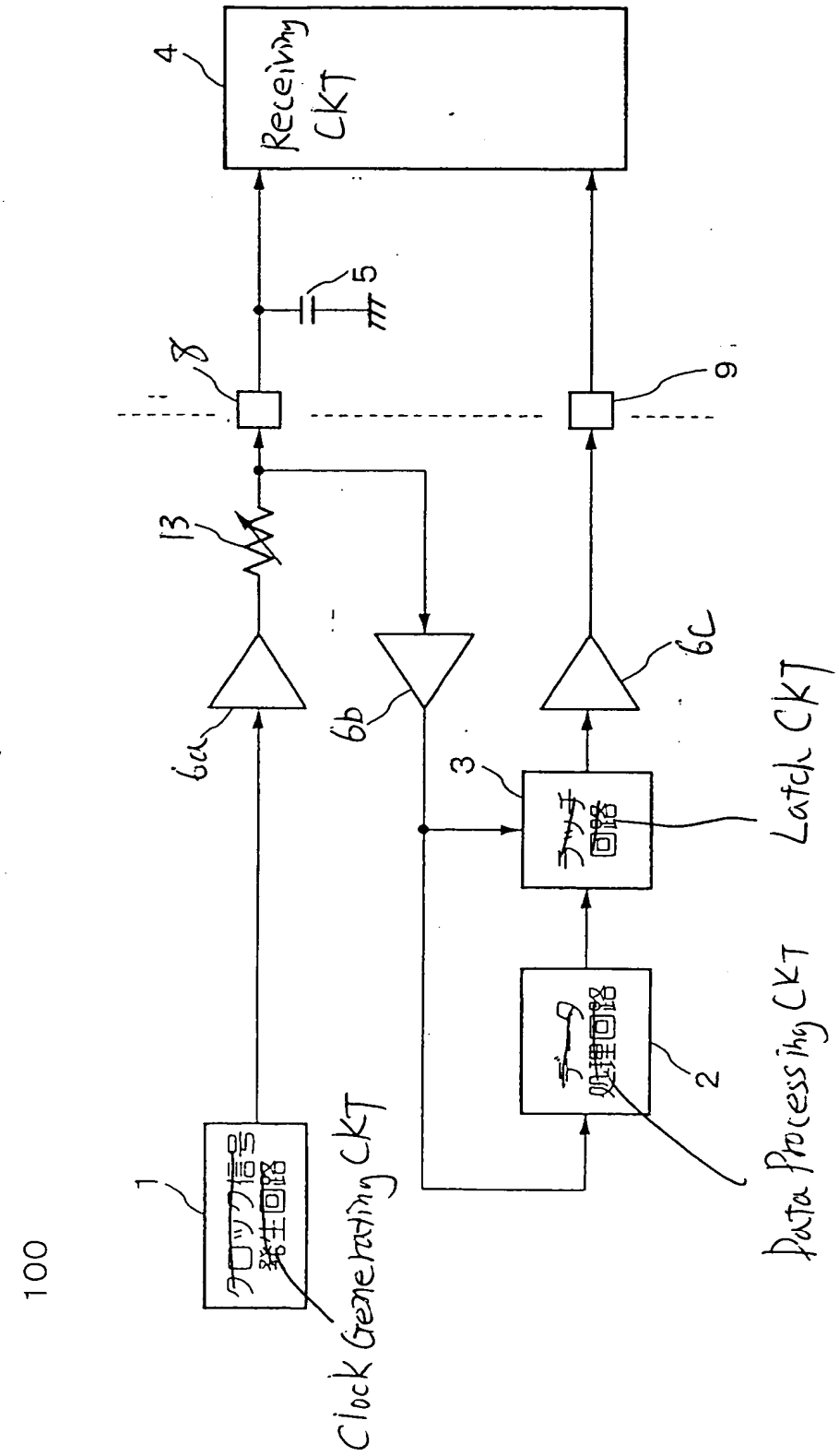

100
Clock Generating CKT
クロック信号発生回路
1
4
Receiving CKT
5
8
9
6a
6b
6c
3
Latch CKT
Data Processing CKT
2
12
11
7

FIG. 3

【図４】

FIG4


4
Receiving CKT
5
8
9
13
6a
6b
6c
3
ラッチ回路
Latch CKT
データ処理回路
2
Data Processing CKT
1
クロック信号発生回路
Clock Generating CKT
100

【図５】

FIG. 5A

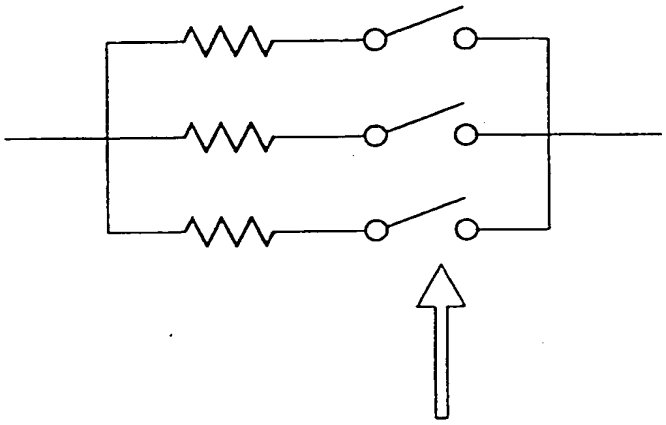
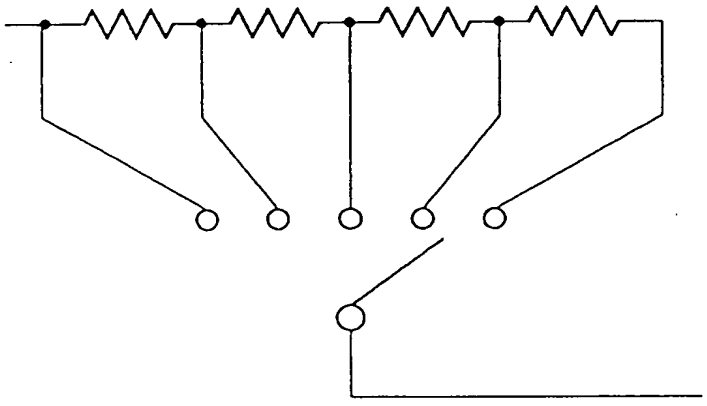


FIG. 5B



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【図6】

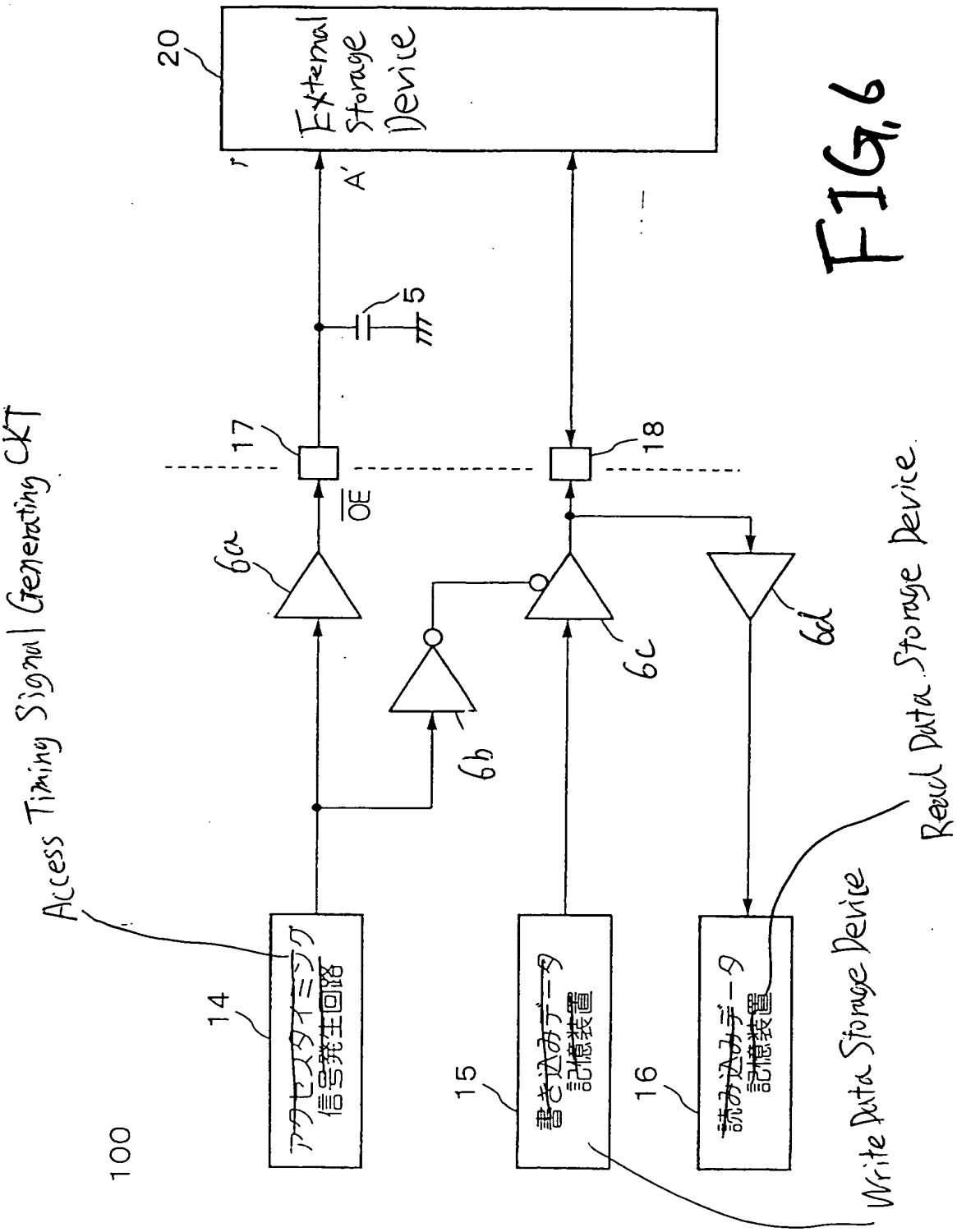

FIG. 6

~~【図7】~~

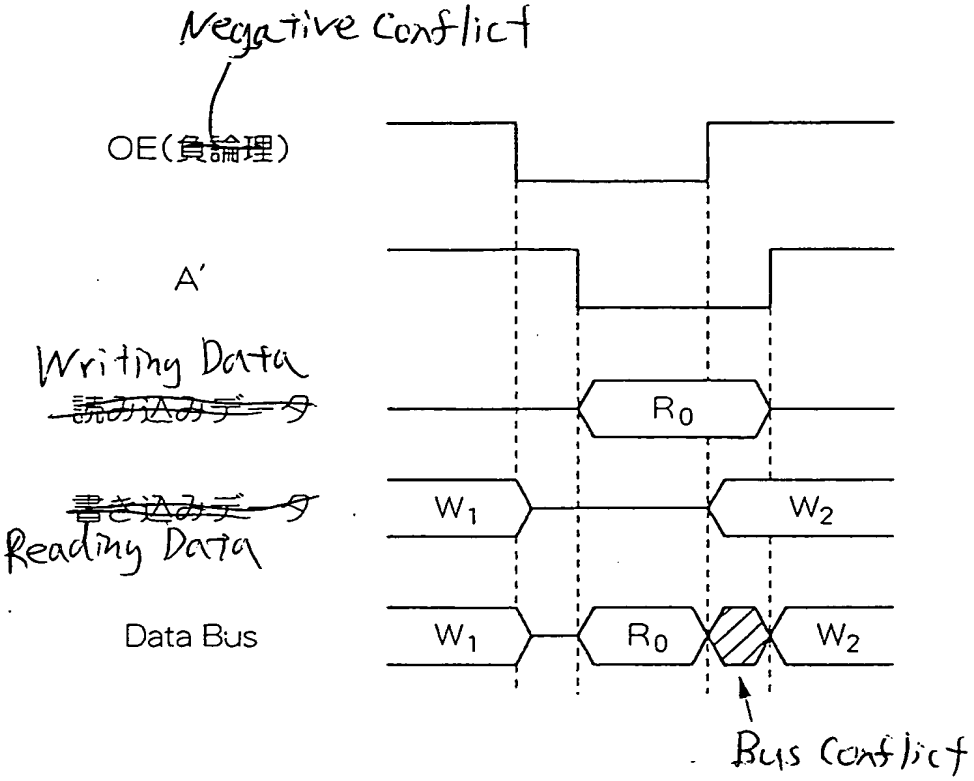
Negative Conflict
OE(負論理)
A'
Writing Data
~~読み込みデータ~~
R0
~~書き込みデータ~~
Reading Data
W1
W2
Data Bus
W1
R0
W2
Bus Conflict

FIG. 7

~~【図8】~~

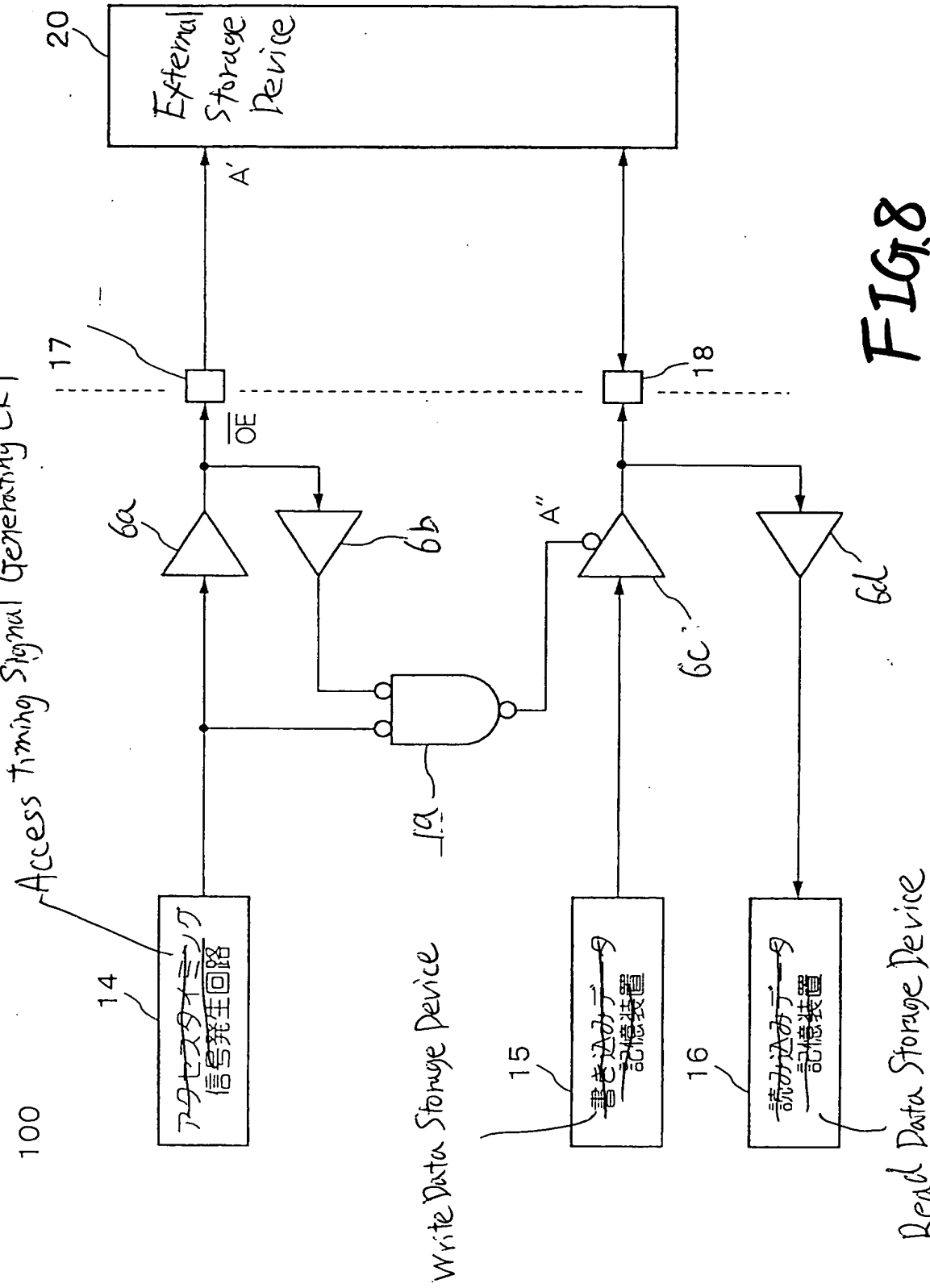
20
External Storage Device
A'
17
18
OE
6a
6b
6c'
6d
A''
19
Access timing Signal Generating CKT
100
14
アクセスタイミング信号発生回路
15
書き込みデータ記憶装置
16
読み込みデータ記憶装置
Write Data Storage Device
Read Data Storage Device

FIG 8

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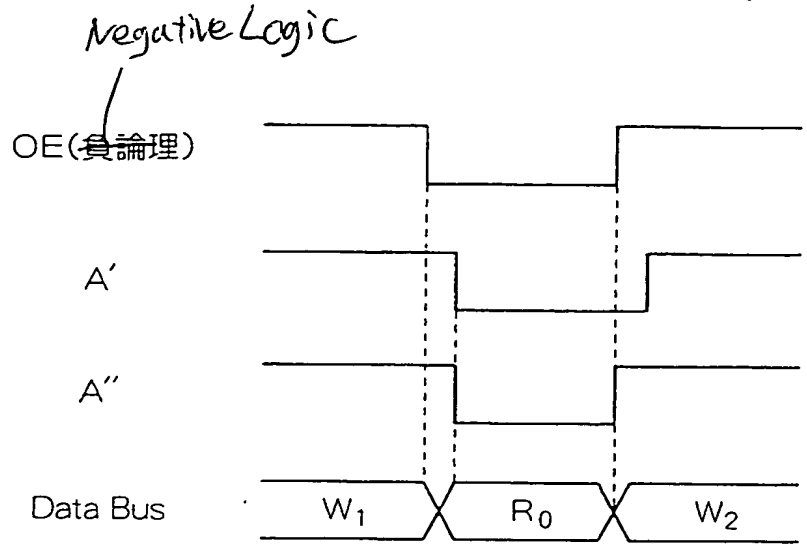
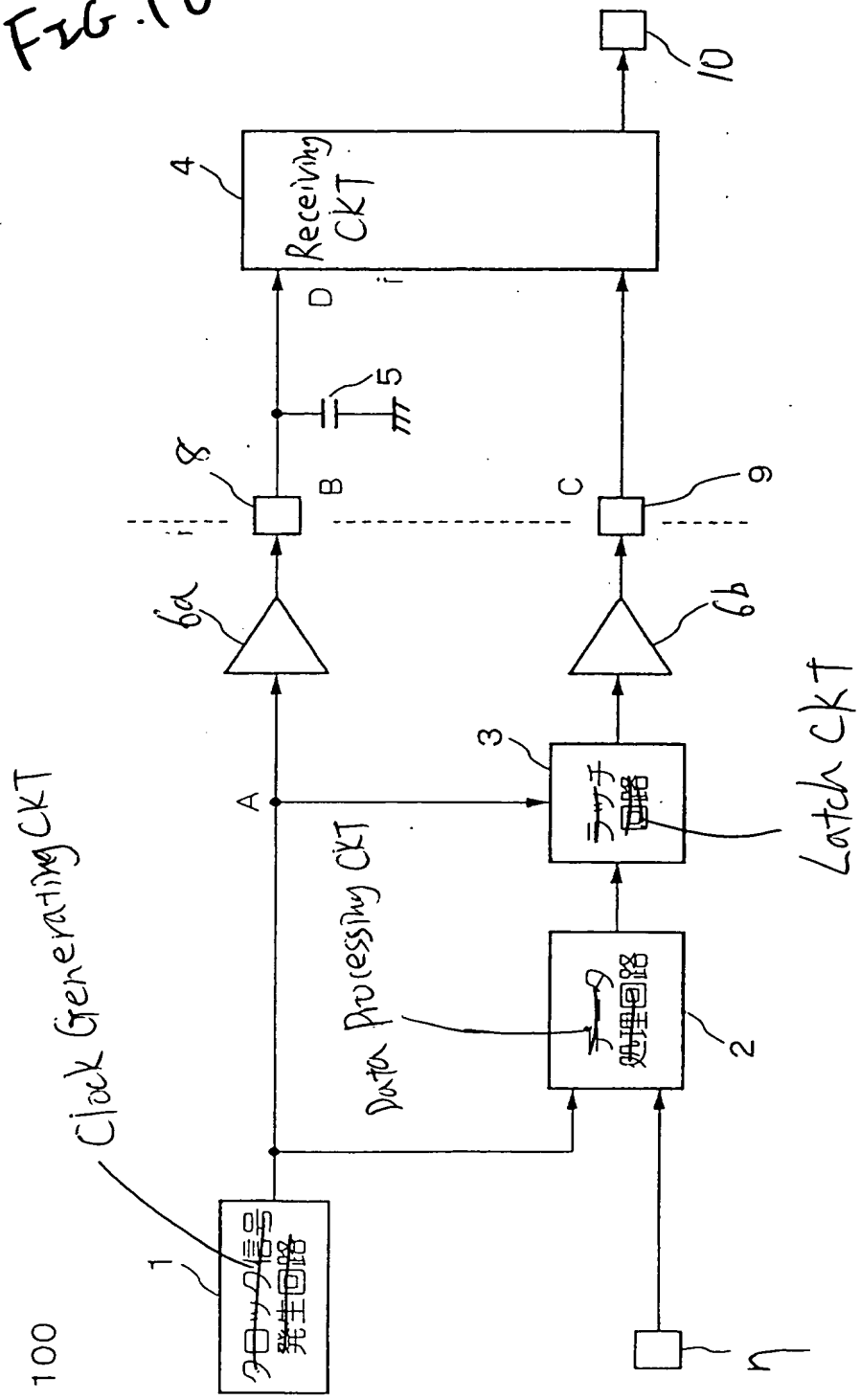
【図9】

FIG. 9



~~【図１０】~~

FIG.10


100
1
クロック信号発生回路
Clock Generating CKT
A
Data Processing CKT
2
データ処理回路
3
ラッチ回路
Latch CKT
6a
6b
B
C
D
5
8
9
4
Receiving CKT
10
11

【図１１】

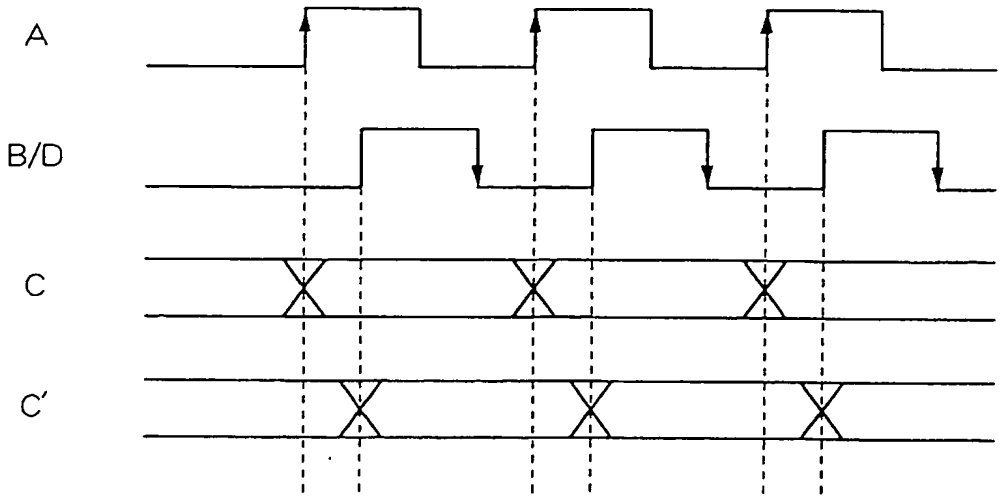


FIG.11